

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/87	Serial No. 10/501,903
	Applicant(s) Martin Vorbach et al.	
	Filing Date March 1, 2005	Group Art Unit 2193

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	60/109,417	November 18, 1998	Jefferson et al.			
	4,571,736	February 18, 1986	Agrawal et al.			
	4,686,386	August 11, 1987	Tadao			
	4,959,781	September 25, 1990	Rubenstein et al.			
	5,287,532	February 15, 1994	Hunt			
	5,408,643	April 18, 1995	Katayose			
	5,412,795	May 2, 1995	Larson			
	5,477,525	December 19, 1995	Masanobu Okabe			
	5,525,971	June 11, 1996	Flynn			
	5,675,757	October 7, 1997	Davidson et al.			
	5,694,602	December 2, 1997	Smith			
	5,706,482	January 6, 1998	Matsushima et al.			
	5,745,734	April 28, 1998	Craft et al.			
	5,801,958	September 1, 1998	Dangelo et al.			
	5,815,726	September 29, 1998	Cliff			
	5,860,119	January 12, 1999	Dockser			
	6,035,371	March 7, 2000	Magloire			
	6,055,619	April 25, 2000	North et al.			
	6,076,157	June 13, 2000	Borkenhagen et al.			
	6,118,724	September 12, 2000	Higginbottom			
	6,188,650	February 13, 2001	Hamada et al.			
	6,247,147	June 12, 2001	Beenstra et al.			
	6,266,760	July 24, 2001	DeHon et al.			
	6,421,808	July 16, 2002	McGeer			
	6,426,649	July 30, 2002	Fu et al.			
	6,483,343	November 19, 2002	Faith et al.			
	6,507,898	January 14, 2003	Gibson et al.			
	6,507,947	January 14, 2003	Schreiber et al.			
	6,538,470	March 25, 2003	Langhammer et al.			
	6,539,438	March 25, 2003	Ledzius et al.			
	6,665,758	December 16, 2003	Frazier et al.			
	6,748,440	June 8, 2004	Lisitsa et al.			
	6,802,026	October 5, 2004	Patterson et al.			
	6,868,476	March 22, 2005	Rosenbluth			
	7,028,107	April 11, 2006	Vorbach et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/87	Serial No. 10/501,903
	Applicant(s) Martin Vorbach et al.	
	Filing Date March 1, 2005	Group Art Unit 2193

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	7,038,952	May 2, 2006	Zack et al.			
	7,043,416	May 9, 2006	Lin			
	7,216,204	May 8, 2007	Rosenbluth			
	7,346,644	March 18, 2008	Langhammer et al.			
	7,595,659	September 29, 2009	Vorbach et al.			
	7,650,448	January 19, 2010	Vorbach et al.			
	2001/0003834	June 14, 2001	Shimonishi			
	2001/ 018733	October 18, 2001	Fujii et al.			
	2002/013861	August 30, 2001	Adiletta et al.			
	2002/124238	September 5, 2002	Metzgen			
	2004/0078548	April 22, 2004	Claydon et al.			
	2009/0085603	April 2, 2009	Paul et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	1 115 204	July 11, 2001	EPO				
	198 22 776	March 25, 1999	Germany			Abstract	
	2 304 438	March 19, 1997	United Kingdom				
	WO 00/045282	August 3, 2000	PCT				
	WO 03/091875	November 6, 2003	PCT				
	1-229378	September 13, 1989	Japan			Abstract	
	6-266605	September 22, 1994	Japan			Abstract	
	7-086921	March 31, 1995	Japan			Abstract	
	8-101761	April 16, 1996	Japan			Abstract	
	8-102492	April 16, 1996	Japan			Abstract	
	8-148989	June 7, 1995	Japan			Abstract	
	8-221164	August 30, 1996	Japan			Abstract	
	9-294069	November 11, 1997	Japan			Abstract	
	2000-076066	March 14, 2000	Japan			Abstract	
	2000-311156	November 7, 2000	Japan			Abstract	
	2001-167066	June 22, 2001	Japan			Abstract	
	11-184718	July 9, 1999	Japan			Abstract	
	5-265705	October 15, 1993	Japan			Abstract	

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/87	Serial No. 10/501,903
	Applicant(s) Martin Vorbach et al.	
	Filing Date March 1, 2005	Group Art Unit 2193

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Advanced RISC Machines, "Introduction to AMBA," October 1996, Section 1, pp. 1-7.
	ARM, "The Architecture for the Digital World," http://www.arm.com/products/ March 18, 2009, 3 pages.
	ARM, "The Architecture for the Digital World; Milestones," http://www.arm.com/aboutarm/milestones.html March 18, 2009, 5 pages.
	Altera, "APEX 20K Programmable Logic Device Family," Altera Corporation Data Sheet, March 2004, ver. 5.1, pp. 1-117.
	Asari, K. et al., "FeRAM circuit technology for system on a chip," <i>Proceedings First NASA/DoD Workshop on Evolvable Hardware</i> (1999), pp. 193-197.
	Becker, J., "Configurable Systems-on-Chip (CSoC)," (Invited Tutorial), Proc. of 9th Proc. of XV Brazilian Symposium on Integrated Circuit, Design (SBCCI 2002), (September 2002).
	Becker et al., "Automatic Parallelism Exploitation for FPL-Based Accelerators," 1998, Proc. 31 st Annual Hawaii International Conference on System Sciences, pp. 169-178.
	Cardoso, J.M.P., et al., "Compilation and Temporal Partitioning for a Coarse-Grain Reconfigurable Architecture," <i>New Algorithms, Architectures and Applications for Reconfigurable Computing</i> , LYSACHT, P. & ROSENTIEL, W. eds., (2005) pp. 105-115.
	Cardoso, J.M.P., et al., "Macro-Based Hardware Compilation of Java™ Bytecodes into a Dynamic Reconfigurable Computing System," <i>IEEE</i> , 21 April 1999, pp.2-11.
	Chaudhry, G.M. et al., "Separated caches and buses for multiprocessor system," <i>Circuits and Systems</i> , 1993; <i>Proceedings of the 36th Midwest Symposium on Detroit, MI, USA, 16-18 August 1993</i> , New York, NY IEEE, 16 August 1993, Pages 1113-1116, XP010119918 ISBN: 0-7803-1760-2.
	Culler, D.E; Singh, J.P., "Parallel Computer Architecture," Pages 434-437, 1999, Morgan Kaufmann, San Francisco, CA USA, XP002477559.
	Cook, Jeffrey J., "The Amalgam Compiler Infrastructure," Thesis at the University of Illinois at Urbana-Champaign (2004) Chapter 7 & Appendix G.
	Del Corso et al., "Microcomputer Buses and Links," Academic Press Inc. Ltd., 1986, pp. 138-143, 277-285.
	Fawcett, B.K., "Map, Place and Route: The Key to High-Density PLD Implementation," <i>Wescon Conference</i> , IEEE Center (7 November 1995) pp. 292-297.
	Hendrich, N., et al., "Silicon Compilation and Rapid Prototyping of Microprogrammed VLSI-Circuits with MIMOLA and SOLO 1400," <i>Microprocessing & Microprogramming</i> (September 1992) vol. 35(1-5), pp. 287-294.
	"IEEE Standard Test Access Port and Boundary-Scan Architecture," <i>IEEE Std. 1149.1-1990</i> , 1993, pp. 1-127.
	Jantsch, Axel et al., "Hardware/Software Partitioning and Minimizing Memory Interface Traffic," <i>Electronic System Design Laboratory</i> , Royal Institute of Technology, ESDLab, Electrum 229, S-16440 Kista, Sweden (April 1994), pp. 226-231.
	Kanter, David, "NVIDIA's GT200: Inside a Parallel Processor," http://www.realworldtech.com/page.cfm?ArticleID=RWTO90989195242&p=1 , September 8, 2008, 27 pages.
	Koch, Andreas et al., "High-Level-Language Compilation for Reconfigurable Computers," <i>Proceedings of European Workshop on Reconfigurable Communication-Centric SOCS</i> (June 2005) 8 pages.
	Lange, H. et al., "Memory access schemes for configurable processors," <i>Field-Programmable Logic and Applications</i> , International Workshop, FPL, 27 August 2000, pages 615-625, XP02283963.
	Lee, R. B., et al., "Multimedia extensions for general-purpose processors," <i>IEEE Workshop on Signal Processing Systems, SIPS 97 - Design and Implementation</i> (1997), pp. 9-23.
	Lee, Ming-Hau et al., "Designs and Implementation of the MorphoSys Reconfigurable Computing Processors," <i>The Journal of VLSI Signal Processing</i> , Kluwer Academic Publishers, BO, Vol. 24, No. 2-3, 2 March 2000, pp. 1-29.
	Mei, Bingfeng et al., "Adres: An Architecture with Tightly Coupled VLIW Processor and Coarse-Grained Reconfigurable Matrix," <i>Proc. Field-Programmable Logic and Applications</i> (FPL 03), Springer, 2003, pp. 61-70.
	Moraes, F., et al., "A Physical Synthesis Design Flow Based on Virtual Components," <i>XV Conference on Design of Circuits and Integrated Systems</i> (November 2000) 6 pages.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/87	Serial No. 10/501,903
	Applicant(s) Martin Vorbach et al.	
	Filing Date March 1, 2005	Group Art Unit 2193

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Neumann, T., et al., "A Generic Library for Adaptive Computing Environments," Field Programmable Logic and Applications, 11 th International Conference, FPL 2001, Proceedings (Lecture Notes in Computer Science, vol. 2147) (2001) pp. 503-512.
	PCI Local Bus Specification, Production Version, Revision 2.1, Portland, OR, June 1, 1995, pp.1-281.
	Piotrowski, A., "IEC-BUS, Die Funktionsweise des IEC-Bus und seine Anwendung in Geräten und Systemen," 1987, Franzis-Verlag GmbH, München, pp. 20-25. [ENGLISH ABSTRACT PROVIDED]
	Pirsch, P. et al., "VLSI implementations of image and video multimedia processing systems," <i>IEEE Transactions on Circuits and Systems for Video Technology</i> , vol. 8, no. 7, Nov. 1998, pp. 878-891.
	Ryo, A., "Auszug aus Handbuch der Informationsverarbeitung," ed. Information Processing Society of Japan, <i>Information Processing Handbook, New Edition</i> , Software Information Center, Ohmsha, December 1998, 4 pages. [Translation provided]
	Salefski, B. et al., "Re-configurable computing in wireless," <i>Annual ACM IEEE Design Automation Conference: Proceedings of the 38th conference on Design automation</i> (2001) pp. 178-183.
	Schmidt, U. et al., "Datawave: A Single-Chip Multiprocessor for Video Applications," <i>IEEE Micro</i> , vol. 11, no. 3, May/June 1991, pp. 22-25, 88-94.
	Schmit, et al., "Hidden Markov Modeling and Fuzzy Controllers in FPGAs, FPGAs for Custom Computing Machines," 1995; Proceedings, IEEE Symposium in Napa Valley, CA, April 1995, pp. 214-221.
	Schönfeld, M., et al., "The LISA Design Environment for the Synthesis of Array Processors Including Memories for the Data Transfer and Fault Tolerance by Reconfiguration and Coding Techniques," <i>J. VLSI Signal Processing Systems for Signal, Image, and Video Technology</i> , 1 October 1995, Vol. 11(1/2), pp. 51-74.
	Shin, D., et al., "C-based Interactive RTL Design Methodology," Technical Report CECS-03-42 (December 2003) pp. 1-16.
	Sondervan, J., "Retiming and logic synthesis," <i>Electronic Engineering</i> (January 1993) vol. 65(793), pp. 33, 35-36.
	XILINX, "The Programmable Logic Data Book," 1994, Section 2, pp.1-231, Section 8, pp. 1, 23-25, 29, 45-52, 169-172.
	XILINX, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays," (v2.2) September 10, 2002, Xilinx Production Product Specification, pp. 1-52.
	XILINX, "Virtex-II and Virtex-II Pro X FPGA Platform FPGAs: Complete Data Sheet," (v4.6) March 5, 2007, pp. 1-302.
	XILINX, "Virtex-II Platform FPGAs: Complete Data Sheet," (v3.5) November 5, 2007, pp. 1-226.
EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	